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Abstract
The development of VLSI design nowadays is mainly focused on low power consumption. With the evolution of CMOS process, device sizes and power supply are also improved. The transistor counts within a chip system is increasing due to huge demand of memory size. In this paper, we try to study memories which occupied a lot of layout area.
The decreasing of device sizes introduces many unpredictable problems such as static power dissipation. Thus, we propose 3 static random access memory architectures with the advantages of low dynamic/static power dissipation. The proposed designs does prove its improvements after we compete with prior design.
As to chip read/write operation, the power consumption in charge/discharge operation of bit line during read/write period is also crucial. We've add selectable charge bit line design and refine the corrosponding circuits. In addition, we also propose a novel design of address sense circuit which also improves in power consumption and transistor counts.
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